ABSTRACT

A comparator for an analog-to-digital converter comprises an input stage (in_+, in_-, M1, M2) for receiving an input signal; a bipolar latch stage (Q1, Q2; Q1a-b, Q2a-b) coupled to the input stage for performing a latch decision based on the input signal; means for amplifying the latch output (V_a, V_b) to a level suitable for CMOS circuitry; and an output (out_+, out_-). The means for amplifying includes at least one tapping transistor (Q3, Q4) coupled to the latch stage for, depending on the latch decision, tapping a collector current (I_{c2}; I_{c1}) from the latch stage, while leaving the latch decision thereof unaffected, such that a current gain (β) of the latch stage can be used to amplify a latch bias current (I_a, I_b) of the latch stage to thereby provide for the amplification.